IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/678,523	Confirmation No. 1345
Applicant	:	Sorel HOROVITZ	
Filed	:	October 3, 2003	
Title	:	METHOD AND APPARATUS FOR FINDING THE NEXT FREE BIT IN A REGISTER	
TC/A.U.	:	2193	
Examiner	:	Chat C. DO	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

The above-identified application having been finally rejected in the Office Action mailed September 10, 2007, Applicant respectfully submits this Pre-Appeal Brief Request for Review within three months of the mailing date of the Office Action (November 10 having fallen on a Saturday, and November 12 being a Federal holiday).

Applicant requests the review for the reason(s) stated on the attached sheets. No amendments are being filed with this request.

A Notice of Appeal is being submitted concurrently herewith.

REMARKS/ARGUMENTS

Claims 7, 11-14, 19, 20, 22-25, 29-37, 39-42, 46-53, 70, 74-77, and 82 are being examined on the merits in the present application. The remainder of claims 1-96 are withdrawn from consideration pursuant to Applicant's Response to the Examiner's Restriction Requirement/Election of Species.

The Examiner has rejected all of the pending claims under 35 U.S.C. § 101. The Examiner has rejected claims 7, 11, 13, 20, 22, 29-31, 33, 36-37, 39, 46-48, 50, 53, 70, 74, and 76 under 35 U.S.C. § 102(a) as anticipated by USP 6,477,552 (Ott '552). The Examiner also has rejected claims 19, 23-24, 35, 40-41, 52, and 82 under 35 U.S.C. § 103(a) as unpatentable over Ott in view of USP 6,697,828 (Ott '828). Applicant respectfully traverses all of these rejections, and requests reconsideration and allowance of the claims in view of the following arguments.

In finally rejecting the claims under 35 U.S.C. § 101, and in pointing to Applicant's remarks bridging pages 3 and 4, the Examiner failed to note that, right at the beginning of those remarks, Applicant stated, "[F]inding a free bit in a register necessarily involves interacting with a hardware apparatus to find a bit. Clearly there is something physical, concrete, or tangible entailed in all of these elected claims." This alone should be sufficient for the claims to be statutory under 35 U.S.C. § 101.

The Examiner also failed to state why Applicant's stated purpose for the claimed invention – to find a place to put a free bit – is not a practical/physical application. The Examiner said only that the purpose is not clearly seen in the claims or in the specification. However, it seems very straightforward that the ordinarily skilled artisan, looking at the claims,

would see a practical and useful purpose for the invention, which is exactly as Applicant stated it: finding a place in a register to put a bit.

As stated in the response to the first Office Action, then, one or more useful purposes for the claimed invention clearly are discernible from the claims. Therefore, Applicant submits that all of the pending claims in the pending application recite statutory subject matter under 35 U.S.C. § 101.

Concerning the prior art rejections, there appears to be a fundamental misunderstanding of what a "free bit in a register" is. The Examiner has equated a zero in an operand to a free bit in a register. Such clearly is not the case. There may be leading zeroes in operands, or zeroes within operands, but that does not in any way equate to identifying a free bit in a register. Even assuming *arguendo*, as the Examiner apparently has done, for example, that the priority encoder 24 in Fig. 2 of Ott '552 is something that selects a zero, that in no way makes that zero a free bit in a register.

A zero in an operand has a purpose. The absence of a "one" bit in a register merely indicates that there is no bit there, not that the value has any meaning or purpose.

Moreover, if one were to take the results of Ott and stick a one, for example, in place of a zero in an operand, the operand is going to change. Nothing in either Ott reference suggests that that is something that the performance of a leading zero determination is intended to do, nor does the Ott apparatus do that inherently, much less explicitly. Neither Ott reference is looking to change the operand – all they are trying to do is to identify leading zeroes.

Consequently, Applicant submits that nothing in either Ott reference, taken alone or in combination, expressly or inherently discloses, or even remotely suggests, that what Ott is trying to do, or inherently does, is to find a free bit in a register. At most, Ott is finding a zero in an operand, which as explained above is not the same thing as finding a place to store a bit.

Moreover, with respect to at least claims 19, 23, 35, 40,52, and 82, and hence their dependent claims 24 and 41, the Examiner has given no reason or motivation whatsoever for combining Ott '552 with Ott '828. Both of these references are concerned with finding leading zeroes in operands. However, that is not enough to justify combining the teachings of the references. There still must be something that Ott '828 adds to Ott '552 that would motivate the ordinarily skilled artisan to pick the portion of Ott '828's Figure 3 structure and somehow add it to the structure of Ott '552. Moreover, the Examiner has not indicated in any way how those two structures can or should be combined to yield the claimed invention.

CONCLUSION

Pursuant to the foregoing, Applicant respectfully requests that the Examiner's rejections be withdrawn. Applicant believes the claims are in condition for allowance. The Commissioner is authorized to charge any fees or credit any overpayment to the deposit account of Kenyon & Kenyon LLP, Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON LLP

Dated: November 13, 2007

By: /Frank L. Bernstein/
Frank L. Bernstein
Reg. No. 31,484

Customer No. **44990**

KENYON & KENYON LLP
333 West San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7500
Facsimile: (408) 975-7501